AS Thematic meeting - project updates

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210924
Updates

- **Two fully equipped FEBs received (all eight chips mounted)**
  - PLL locking successful on all 8 chips x 2 boards.
  - Coincidence testing on 256 channel setup tested.
  - Optimization in progress

- **DAQ**
  - Firmware update: unbiased GMSL representation
  - Maximum rate up to 2M.counts.s⁻¹, further optimization to increase ~10Mcps.
  - Global Reset implemented
  - in collaboration with CH, ML, WC, Coco

- **Mechanics**
  - Connector for increased spacing
  - Gluing protocol developed; tested on PE+PMMA; detector modules are being prepared.
  - Al plate for dissipating the heat generated on the ASIC - designed, fabricated and tested

- **Software GUI development**
  - Channel maps, visualization of local and global information
  - in collaboration with YC

- **Gamma detector R&D**
  - Beam test analysis by C Tran
  - Other investigations on Knife edge collimation by V Sihotang

- **Timeline**
Introduction

The FT600 and FT601, collectively referred to as FT60x, are designed to bridge USB packets from USB2.0 and USB3.0 hosts to a USB function through a FIFO interface. The bridge implements the FIFO slave interface which may be configured as a FT245 (single channel) or FT600 (multi-channel) bus.

In typical designs, an FPGA is used to implement the FIFO master interface to communicate with the bridge. The FPGA and other devices (not shown) implement the remaining features of the target USB function(s).

The bridge handles all USB related configuration, control and data transfer and simplifies customer designs that require an USB2.0/USB3.0 device port.

Figure 1 - FT60x System Block Diagram
Before USB board firmware upgrade:
Biased GMSL representation

210720

After USB board firmware upgrade:
Unbiased GMSL representation

210828

DAQ
Bias in the GMSL addressed
# DAQ

## Measured rate improved

### Previous DAQ rate ~70kHz

### Current DAQ rate ~2.2 MHz (visualization removed)

### Potential DAQ rate ~10MHz (need optimization)

<table>
<thead>
<tr>
<th>DAQ rate overall</th>
<th>Ch</th>
<th>BOARD0</th>
<th>BOARD1</th>
<th>DAQ efficiency</th>
<th>% good events</th>
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<td>FPGA0</td>
<td>FPGA1</td>
<td>FPGA0</td>
<td>FPGA1</td>
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</tbody>
</table>

*Green=ON chip Chip*

Test settings

**Test-pulse rate=1/10.24us (dTcc=6404)**

RST ON rate=1/100us

Expected rate per chip=97.7kHz

Data: 210828/..

Firmware: Test_USB_impl1_210818.jed

Software: 210829

Measured with one or more chips ON, 16 channels

USB3.0 rate limit ~50MHz
DAQ
Global RST

RST

FRAME

EVENT

EVENT
DAQ

Global RST event

- Once every 100us—> a reset is issued to synchronize the counters. This can be used to keep track of the global event timeline.

- Physically there is a unique event called Reset event generated every 20 resets - or - every 2ms.
  - Within the 20 resets, we can keep track of the reset count by reading the bits0-4 of any event - this counter will be incremented for each reset.

- This RST event has unique attributes that can let us identify it.
  - RST event of 64 bits: once every 20 resets (10 kHz RST rate)
  - Marker: Bits 26-55 All-1s (forbidden state for Tcoarse bits)
  - Counter: Bits LSB0-MSB25
  - Counter local: Bits0-4 (for all events; to track RST count between two RST events)
  - Address: Bits 56-63 (to identify the board, gmsl, stic ids)

*Some issues in RST event were identified and fully resolved.
Mechanics

Optical coupling

• SG600 optical cement: resin+hardener

• Quality attributes
  • Alignment
  • Uniformity - air bubble
    • Vacuum for air bubbles (10⁻² Torr) - checked and works
  • Spillage/cleanup
    • Periodic monitoring

• Other solutions investigated:
  • 3M tape 0.5mm
  • Optical grease + mechanical holding by silicone glue solutions
Mechanics

Optical coupling protocol:
8x8 array, 3.2 mm pitch

• Mix the optical cement ~10g

• Vacuum for 5 mins

• Inject in syringe and vacuum for 5 mins

• Apply 0.15g (0.1-0.2g) of optical cement mixture on the crystal within 30 mins of preparation
  • Apply a central blob
  • Place the SiPM gently, self weight spreads the glue
  • Cleanup the sides and align on the alignment frame
Mechanics

Connector board between FEB1 and FEB2

Increased space between FEB1-FEB1 allows for better heat dissipating solutions
Mechanics

Heat dissipation: heat pipe, metal plate

Super pure water circulated in a low pressure pipe enables the extraction of heat by evaporation followed by condensation away from the board with an external fan. \( \sim 10W \) Qmax

Al plate is coupled to the chip using a thermal paste. The heat is dissipated by conduction from the chip to the plate to the side walls. Heatsink can be placed at the last step to dissipate the heat by convection.
Mechanics

Metal plate for heat dissipation

Al cooling plate 3.6mm thick
ASIC surface to Al plate surface: 0.4mm gap
Silicone heat sink paste: Y500 (upto 250C)

Tested on a board with 4 chips arranged in a zig zag configuration

Temperature chamber at 25C
Mechanics

ASIC temperature in various configurations

Temperature chamber at 25°C

- T=51°C
- T=46°C
- T=39°C

Time (s) vs. Temperature

with heat pipe
without fan
with fan
without fan, Cu heat sink
Software: NTU visualization

in collaboration with NTU

- A GUI must be developed to visualize the information contained in the data.

- **One tab** for the detector topology

- **One tab** for the **global hits** as represented within various boardID, gmslID and sticID - selection can be made to further specify the board and/or gmsl to view the counts of sticIDs specific to a given gmsl within a board.

- **One tab** for the local hits as represented by the channel hit map and by a grid of histograms for each stic divided in four subsections (16 channel sets) for ease of viewing.

- **One tab** for reconstructed image
• Next meeting tentative date: **211126**

• October+: Detector assembly, testing and optimization

• November: Prepare for a beam test:
  • range verification with range shifters;
  • simulation of the beam test scenario

• Studies on PG and PAG for novel detectors and applications
Appendix
Gamma activity image reconstructed from the coincidence signals measured by the detector. The radioactive source is moved along the detector axis; a corresponding change in the image (yellow spot) is observed. Source shifts in 1.5 mm steps can be seen in the image to the right.

*Radioactive source is a positron emitting isotope $^{22}$Na which emits coincident gamma with 511 keV energy.
• Current firmware FEB: 210911
• Current firmware USB: 210906
• Current DAQ software: FTD3XX_RevD_210906
• Current Analysis code: BinaryRead9.cpp